Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

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**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: G = .050” X .050” S = .203” X .203”**

**Backside Potential: DRAIN**

**Mask Ref: IX8C**

**APPROVED BY: DK DIE SIZE .282” X .350” DATE: 5/3/17**

**MFG: IXYS THICKNESS .010” P/N: IXTD16N10D2-8C**

**DG 10.1.2**

#### Rev B, 7/1